Amendments to the Specification:

Please replace paragraph [0017], on page 4 of the specification with the following amended paragraph:

Referring to FIG 3, it illustrates a top view of a memory array according to one embodiment of the present invention. Shallow trench isolations (STI) structures 403 are formed parallel to each other in a semiconductor substrate 400. Additionally, a pair of control gates 420 of the split gate effect transistors are formed orthogonally to the STI structures 403. Pairs of floating gates 420 and overlap with the STI structures 403. Finally, source~~/~~ and drain regions 411 and 430 are formed beside the floating gates ~~408~~ 404 and the control gates 420.